



# LPC8N04

32-bit ARM Cortex®-M0+ microcontroller; 32 kB flash and 8 kB SRAM; NFC/RFID ISO 14443 type A interface

Rev. 1.4 — 8 June 2018

Product data sheet

## 1. General description

The NXP LPC8N04 is an IC optimized for an entry level Cortex-M0+ MCU with built-in NFC interface. LPC8N04 supports an effective system solution with a minimal number of external components for NFC related applications.

The embedded ARM Cortex-M0+ offers flexibility to the users of this IC to implement their own dedicated solution. The LPC8N04 contains multiple features, including multiple power-down modes and a selectable CPU frequency of up to 8 MHz, for ultra-low power consumption.

Users can program this LPC8N04 with the industry-wide standard solutions for ARM Cortex-M0+ processors.

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

### CAUTION



Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.



## 2. Features and benefits

- System
  - ◆ ARM Cortex-M0+ processor running at frequencies of up to 8 MHz
  - ◆ ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC)
  - ◆ ARM Serial Wire Debug (SWD)
  - ◆ System tick timer
  - ◆ IC reset input
- Memory
  - ◆ 32 kB on-chip flash programming memory
  - ◆ 4 kB on-chip EEPROM of which 256 byte can be write protected
  - ◆ 8 kB SRAM
- Digital peripherals
  - ◆ Up to 12 General Purpose Input Output (GPIO) pins with configurable pull-up/pull-down resistors and repeater mode
  - ◆ GPIO pins which can be used as edge and level sensitive interrupt sources
  - ◆ High-current drivers/sinks (20 mA) on four GPIO pins
  - ◆ High-current drivers/sinks (20 mA) on two I<sup>2</sup>C-bus pins
  - ◆ Programmable WatchDog Timer (WDT)
- Analog peripherals
  - ◆ Temperature sensor with  $\pm 1.5$  °C absolute temperature accuracy between –40 °C and +85 °C
- Communication interfaces
  - ◆ NFC/RFID ISO 14443 type A interface
  - ◆ I<sup>2</sup>C-bus interface supporting full I<sup>2</sup>C-bus specification and fast mode with a data rate of 400 kbit/s, with multiple address recognition and monitor mode
- Energy harvesting functionality to power the LPC8N04.
- OTA firmware update using Secondary Bootloader (SBL) library (See TN00040: LPC8N04: Encrypted Over the Air (OTA) Firmware update using NFC). OTA firmware update available on Boot ROM version 0.14.
- Clock generation
  - ◆ 8 MHz internal RC oscillator, trimmed to 2 % accuracy, which is used for the system clock
  - ◆ Timer oscillator operating at 32 kHz linked to the RTC timer unit
- Power control
  - ◆ Support for 1.72 V to 3.6 V external voltages
  - ◆ The LPC8N04 can also be powered from the NFC field
  - ◆ Activation via NFC possible
  - ◆ Integrated Power Management Unit (PMU) for versatile control of power consumption
  - ◆ Four reduced power modes for ARM Cortex-M0+: sleep, deep sleep, deep power-down and battery off
  - ◆ Power gating for each analog peripheral for ultra-low power operation
  - ◆ < 50 nA IC current consumption in battery off mode at 3.0 V
  - ◆ Power-On Reset (POR)

- Unique device serial number for identification

### 3. Applications

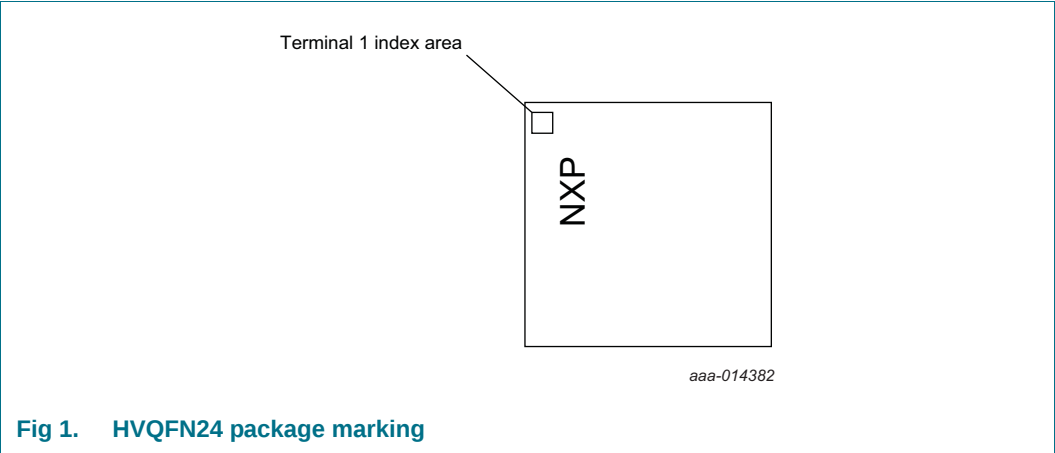
- Configurable LED strip/christmas tree LEDs via NFC
- Smart toy/interactive robot data logger
- Buttonless/contactless control panel
- Contactless diagnostic
- NFC e-locker
- Smart manufacturing
- NFC OTA

### 4. Ordering information

Table 1. Ordering information

| Type number  | Package |                                                                                                    |          |
|--------------|---------|----------------------------------------------------------------------------------------------------|----------|
|              | Name    | Description                                                                                        | Version  |
| LPC8N04FHI24 | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm | SOT616-3 |

### 5. Marking



The LPC8N04 HVQFN24 package has the following top-side marking:

- First line: Syww
  - yww: Date code with y = year and ww = week.
- Second line: xxxx
- Third line: LPC8N04

6. Block diagram

The internal block diagram of the LPC8N04 is shown in [Figure 2](#). It consists of a Power Management Unit (PMU), clocks, timers, a digital computation and control cluster (ARM Cortex-M0+ and memories) and AHB-APB slave modules.

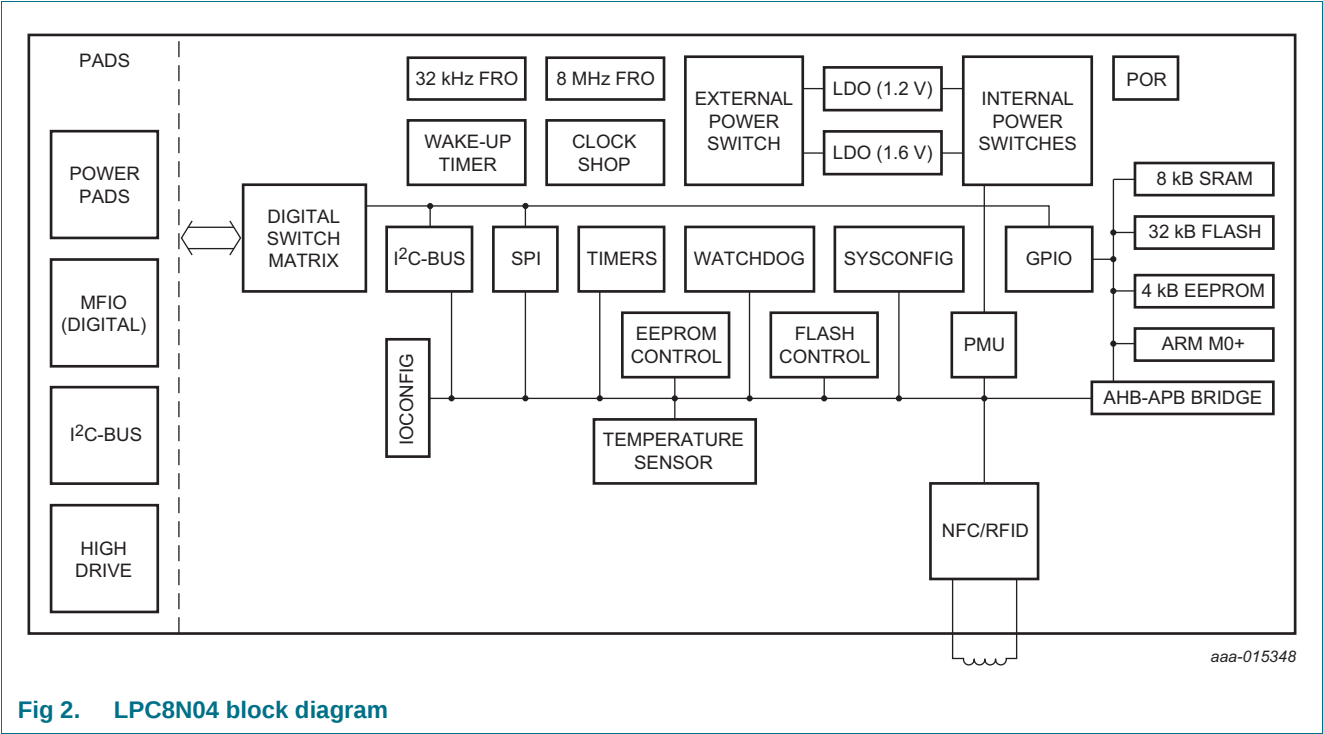


Fig 2. LPC8N04 block diagram

7. Pinning information

7.1 Pinning

7.1.1 HVQFN24 package

Figure 3 shows the pad layout of the LPC8N04 in the HVQFN24 package.

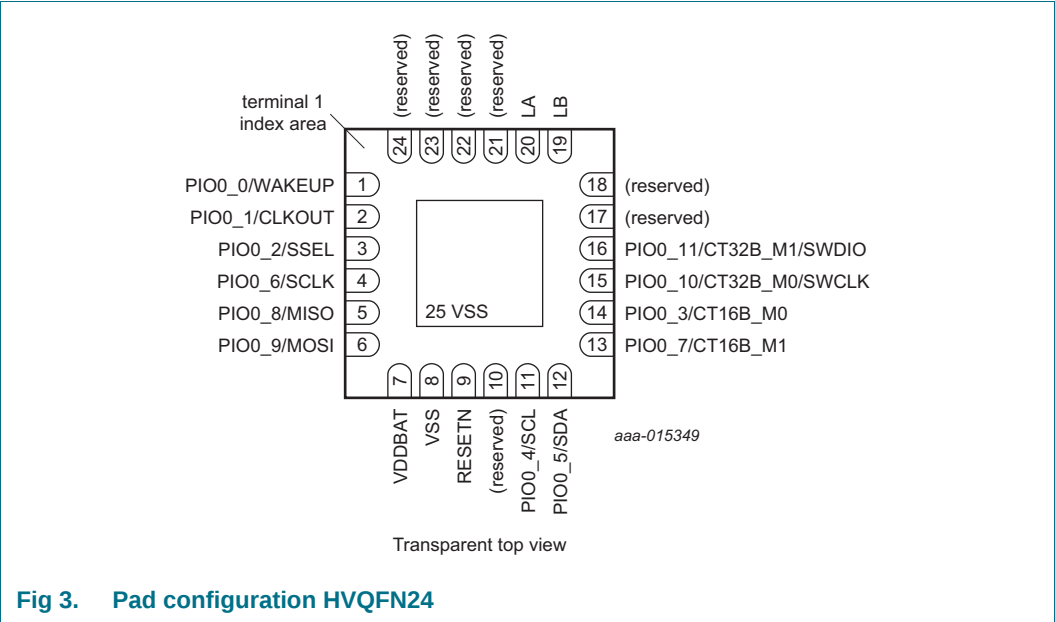


Table 2. Pad allocation table of the HVQFN24 package

| Pad | Symbol        | Pad               | Symbol                 |
|-----|---------------|-------------------|------------------------|
| 1   | PIO0_0/WAKEUP | 13 <sup>[1]</sup> | PIO0_7/CT16B_M1        |
| 2   | PIO0_1/CLKOUT | 14 <sup>[1]</sup> | PIO0_3/CT16B_M0        |
| 3   | PIO0_2/SSEL   | 15 <sup>[1]</sup> | PIO0_10/CT32B_M0/SWCLK |
| 4   | PIO0_6/SCLK   | 16 <sup>[1]</sup> | PIO0_11/CT32B_M1/SWDIO |
| 5   | PIO0_8/MISO   | 17 <sup>[2]</sup> | RESERVED               |
| 6   | PIO0_9/MOSI   | 18 <sup>[2]</sup> | RESERVED               |
| 7   | VDDBAT        | 19                | LB                     |
| 8   | VSS           | 20                | LA                     |
| 9   | RESETN        | 21 <sup>[2]</sup> | RESERVED               |
| 10  | RESERVED      | 22 <sup>[2]</sup> | RESERVED               |
| 11  | PIO0_4/SCL    | 23 <sup>[2]</sup> | RESERVED               |
| 12  | PIO0_5/SDA    | 24 <sup>[2]</sup> | RESERVED               |

[1] High source current pads; see [Section 8.6.3](#).  
[2] These pads must be tied to ground.

Table 3. Pad description of the HVQFN24 package

| Pad                       | Symbol   | Type   | Description                                     |
|---------------------------|----------|--------|-------------------------------------------------|
| <b>Supply</b>             |          |        |                                                 |
| 7                         | VDDBAT   | supply | positive supply voltage                         |
| 8                         | VSS      | supply | ground                                          |
| <b>GPIO<sup>[1]</sup></b> |          |        |                                                 |
| 1                         | PIO0_0   | I/O    | GPIO                                            |
|                           | WAKEUP   | I      | deep power-down mode wake-up pin <sup>[2]</sup> |
| 2                         | PIO0_1   | I/O    | GPIO                                            |
|                           | CLKOUT   | O      | clock output                                    |
| 3                         | PIO0_2   | I/O    | GPIO                                            |
|                           | SSEL     | I      | SPI/SSP serial select line                      |
| 14                        | PIO0_3   | I/O    | GPIO                                            |
|                           | CT16B_M0 | O      | 16-bit timer match output 0                     |
| 11                        | PIO0_4   | I/O    | GPIO                                            |
|                           | SCL      | I/O    | I <sup>2</sup> C-bus SCL clock line             |
| 12                        | PIO0_5   | I/O    | GPIO                                            |
|                           | SDA      | I/O    | I <sup>2</sup> C-bus SDA data line              |
| 4                         | PIO0_6   | I/O    | GPIO                                            |
|                           | SCLK     | I/O    | SPI/SSP serial clock line                       |
| 13                        | PIO0_7   | I/O    | GPIO                                            |
|                           | CT16B_M1 | O      | 16-bit timer match output 1                     |
| 5                         | PIO0_8   | I/O    | GPIO                                            |
|                           | MISO     | O      | SPI/SSP master-in slave-out line                |
| 6                         | PIO0_9   | I/O    | GPIO                                            |
|                           | MOSI     | I      | SPI/SSP master-out slave-in line                |
| 15                        | PIO0_10  | I/O    | GPIO                                            |
|                           | CT32B_M0 | O      | 32-bit timer match output 0                     |
|                           | SWCLK    | I      | ARM SWD clock                                   |
| 16                        | PIO0_11  | I/O    | GPIO                                            |
|                           | CT32B_M1 | O      | 32-bit timer match output 1                     |
|                           | SWDIO    | I/O    | ARM SWD I/O                                     |
| <b>Radio</b>              |          |        |                                                 |
| 20                        | LA       | A      | NFC antenna/coil terminal A                     |
| 19                        | LB       | A      | NFC antenna/coil terminal B                     |
| <b>Reset</b>              |          |        |                                                 |
| 9                         | RESETN   | I      | external reset input <sup>[3]</sup>             |

[1] The GPIO port is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pads depends on the function selected through the IOCONFIG register block.

[2] If external wake-up is enabled on this pad, it must be pulled HIGH before entering deep power-down mode and pulled LOW for a minimum of 100  $\mu$ s to exit deep power-down mode.

[3] A LOW on this pad resets the device. This reset causes I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. It has weak pull-up to V<sub>DDBAT</sub>.

## 8. Functional description

---

### 8.1 ARM Cortex-M0+ core

Refer to the *Cortex-M0+ Devices Technical Reference Manual* ([Ref. 1](#)) for a detailed description of the ARM Cortex-M0+ processor.

The LPC8N04 ARM Cortex-M0+ core has the following configuration:

- System options
  - Nested Vectored Interrupt Controller (NVIC)
  - Fast (single-cycle) multiplier
  - System tick timer
  - Support for wake-up interrupt controller
  - Vector table remapping register
  - Reset of all registers
- Debug options
  - Serial Wire Debug (SWD) with two watchpoint comparators and four breakpoint comparators
  - Halting debug is supported

### 8.2 Memory map

[Figure 4](#) shows the memory and peripheral address space of the LPC8N04.

The only AHB peripheral device on the LPC8N04 is the GPIO module. The APB peripheral area is 512 kB in size. Each peripheral is allocated 16 kB of space.

All peripheral register addresses are 32-bit word aligned. Byte and half-word addressing is not possible. All reading and writing are done per full word.

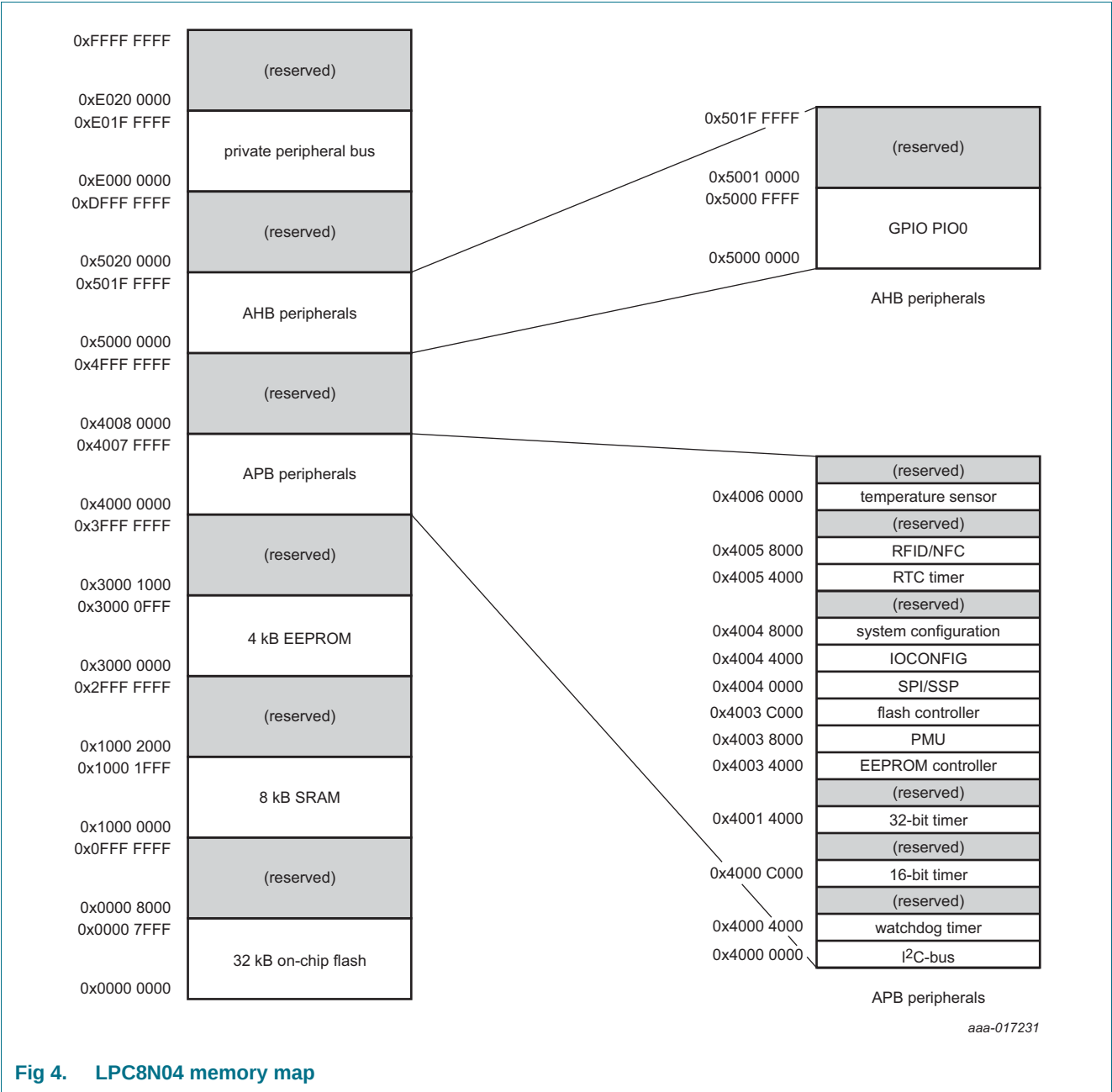


Fig 4. LPC8N04 memory map

8.3 System configuration

The system configuration APB block controls oscillators, start logic and clock generation of the LPC8N04. Also included in this block is a register for remapping the interrupt vector table.

8.3.1 Clock generation

The LPC8N04 Clock Generator Unit (CGU) includes two independent RC oscillators. These oscillators are the System Free-Running Oscillator (SFRO) and the Timer Free-Running Oscillator (TFRO).

The SFRO runs at 8 MHz. The system clock is derived from it and can be set to 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz or 62.5 kHz (Note: some features are not available when using the lower clock speeds). The TFRO runs at 32.768 kHz and is the clock source for the timer unit. The TFRO cannot be disabled.

Following reset, the LPC8N04 starts operating at the default 500 kHz system clock frequency to minimize dynamic current consumption during the boot cycle.

The SYSAHBCLKCTRL register gates the system clock to the various peripherals and memories. The temperature sensor receives a fixed clock frequency, irrespective of the system clock divider settings, while the digital part uses the system clock (AHB clock 0).

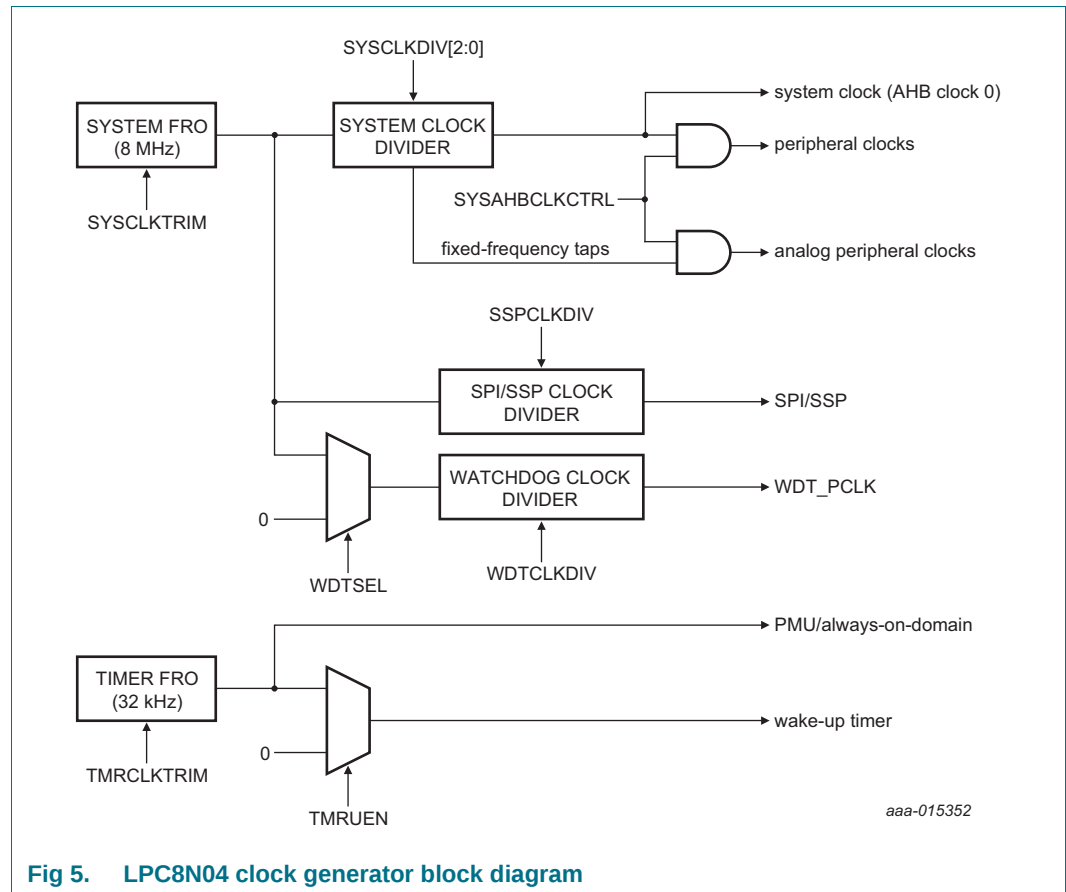


Fig 5. LPC8N04 clock generator block diagram

### 8.3.2 Reset

Reset has three sources on the LPC8N04: the RESETN pin, watchdog reset and a software reset.

## 8.4 Power management

The Power Management Unit (PMU) controls the switching between available power sources and the powering of the different voltage domains in the IC.

### 8.4.1 System power architecture

The LPC8N04 accepts power from two different sources: from the external power supply pin VDDBAT, or from the built-in NFC/RFID rectifier.

The LPC8N04 has a small automatic source selector that monitors the power inputs (VBAT and VNFC, see [Figure 6](#)) as well as pin RESETN. The PSWBAT switch is kept open until a trigger is given on pin RESETN or via the NFC field. If the trigger is given, the always-on domain, VDD\_ALON, itself is powered via the PSWBAT or the PSWNFC switch: via VBAT, if  $VBAT > 1.72\text{ V}$ , or VNFC. Priority is given to VBAT when both VBAT and VNFC are present.

The automatic source selector unit in the PMU decides on the powering of the internal domains based on the power source.

- If a voltage  $> 1.72\text{ V}$  is detected on VBAT and not VNFC, VBAT powers the internal domains after a trigger on pin RESETN or via NFC.
- If a voltage  $\leq 1.72\text{ V}$  is detected on VBAT, and a higher voltage is detected on VNFC, the internal domains are powered from VNFC.
- If a voltage  $> 1.72\text{ V}$  is detected at both VBAT and VNFC, the internal domains are powered from VBAT.
- Switch over between power sources is possible. If initially both VBAT and VNFC are available, the system is powered from VBAT. If VBAT then becomes unavailable (because it is switched off externally, or by a PSWBAT/PSWNFC power switch override), the internal domains are immediately powered from VNFC. Switch over is supported in both directions.
- The user can force the selection of the VBAT input by disabling the automatic power switch, which disables the automatic source selector voltage comparator.

When on NFC power only (passive operation), connecting one or more 100 nF external capacitors in parallel to a GPIO pad, and setting that pad as an output driven to logic 1, is advised. Preferably a high-drive pin should be chosen and several pins can be connected in parallel.

PSWNFC and PSWBAT are the power switches. PSWNFC connects power to the VDD\_ALON power net when an RF field is present. PSWBAT connects power from the battery when a positive edge is detected on RESETN. If no RF power is available, the PMU can open this PSWBAT switch, effectively switching off the device. After connecting VDDBAT to a power source, the PSWBAT switch is open until a rising edge is detected on RESETN or RF power is applied.

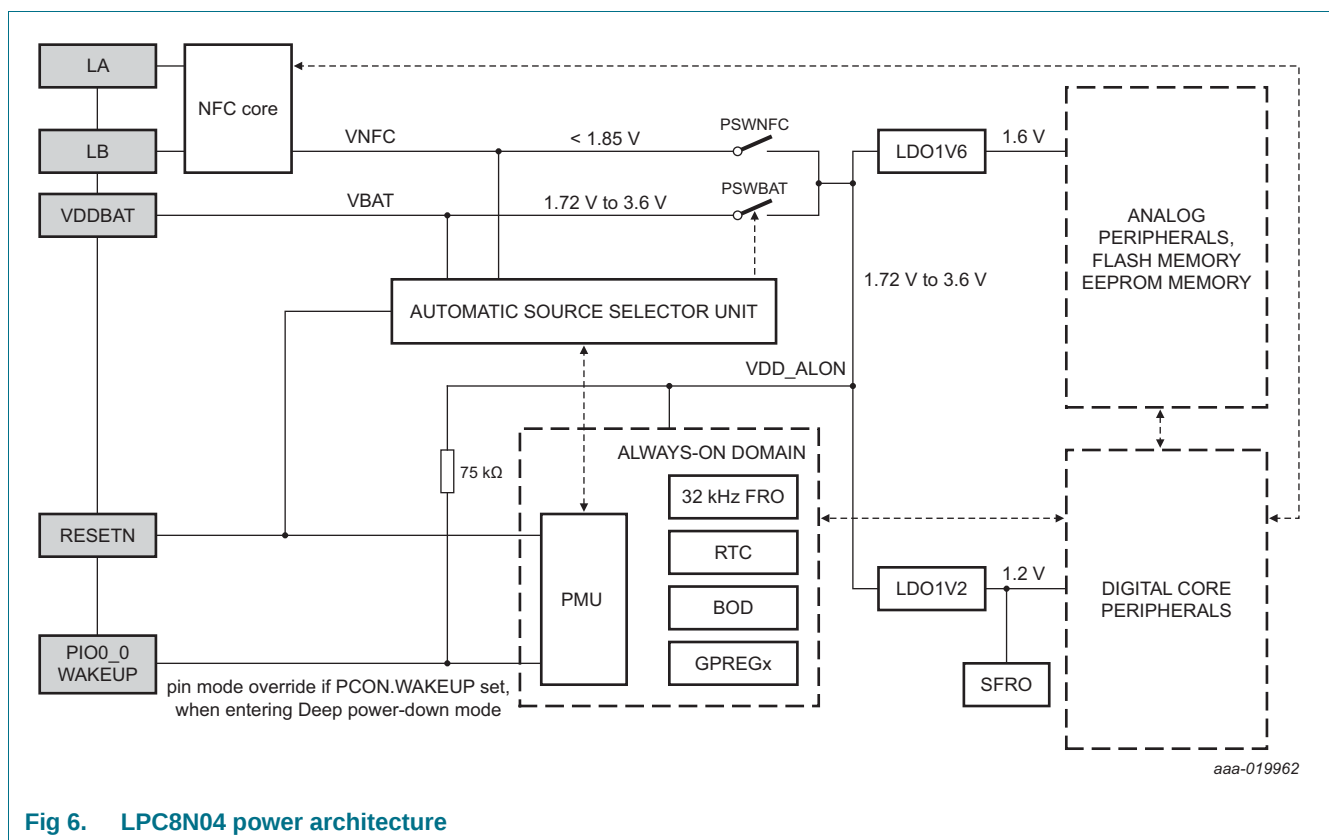
Each component of the LPC8N04 resides in one of several internal power domains, as indicated in [Figure 6](#). The domains are VBAT, VNFC, VDD\_ALON, VDD1V2 and VDD1V6. The domains VDD\_ALON, VDD1V2 and VDD1V6 are powered, or not, depending on the mode of the LPC8N04. There are five modes: active, sleep, deep sleep, deep power-down and battery off.

The VDD\_ALON domain contains BrownOut Detection (BOD). When enabled, if the VDD\_ALON voltage drops below 1.8 V it raises a BOD interrupt.

The PMU controls the active, sleep, deep sleep and deep power-down modes, and thus the power flow to the different internal components.

The PMU has two LDOs powering the internal VDD1V2 and VDD1V6 voltage domains. LDO1V2 converts voltages in the range 1.72 V to 3.6 V into 1.22 V. LDO1V6 converts voltages in the range 1.72 V to 3.6 V into 1.6 V. Each LDO can be enabled separately. A 1.2 nF buffer capacitor is included at the input of the LDOs when powered via VNFC.

The trigger detector (not shown in [Figure 6](#)) and power gate have a leakage of less than 50 nA to allow for long shelf life before activation.



**Fig 6. LPC8N04 power architecture**

The PMU states and settings of the LDOs are summarized in [Table 4](#), and the state transitions are shown in [Figure 7](#).

[Table 5](#) and [Table 6](#) summarize the events that can influence wake-up from deep power-down or deep sleep modes (DEEPPDN or DEEPSLEEP to ACTIVE state transition).

Table 4. IC power states

| State           | VDD_ALON | DPDN <sup>[1]</sup> | Sleep or Deep-sleep | LDO1 1.2 V | LDO2 1.6 V |
|-----------------|----------|---------------------|---------------------|------------|------------|
| NOPOWER         | no       | X <sup>[2]</sup>    | X <sup>[2]</sup>    | off        | off        |
| ACTIVE          | yes      | 0                   | 0                   | on         | on         |
| DEEPPDN         | yes      | 1                   | 0                   | off        | off        |
| SLEEP/DEEPSLEEP | yes      | 0                   | 1                   | on         | on         |

[1] DPN indicates whether the system is in deep power-down mode.

[2] X = don't care.

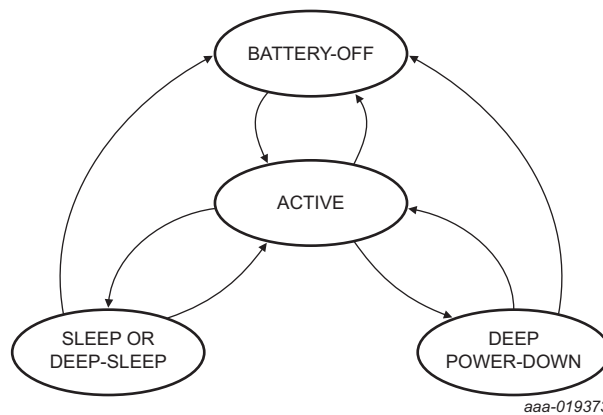


Fig 7. PMU state transition diagram

The power-up sequence is shown in [Figure 8](#). Applying battery power when the PSWBAT switch is closed, or NFC power becomes available, provides the always-on part with a Power-On Reset (POR) signal. The TFRO is initiated which starts a state machine in the PMU. In the first state, the LDO1V2 powering the digital domain is started. In the second state, the LDO1V6 powering the analog domain is started which starts the flash memory. Enabling the LDO1V2, and the SFRO stabilizing, triggers the system\_por. The system is now considered to be 'on'. The system can boot when the flash memory is fully operational.

The total start-up time from trigger to active mode/boot is about 2.5 ms.

If there is no battery power, but there is RF power, the same procedure is followed except that PSWNFC connects power to the LDOs.

The user cannot disable the TFRO as it is used by the PMU.

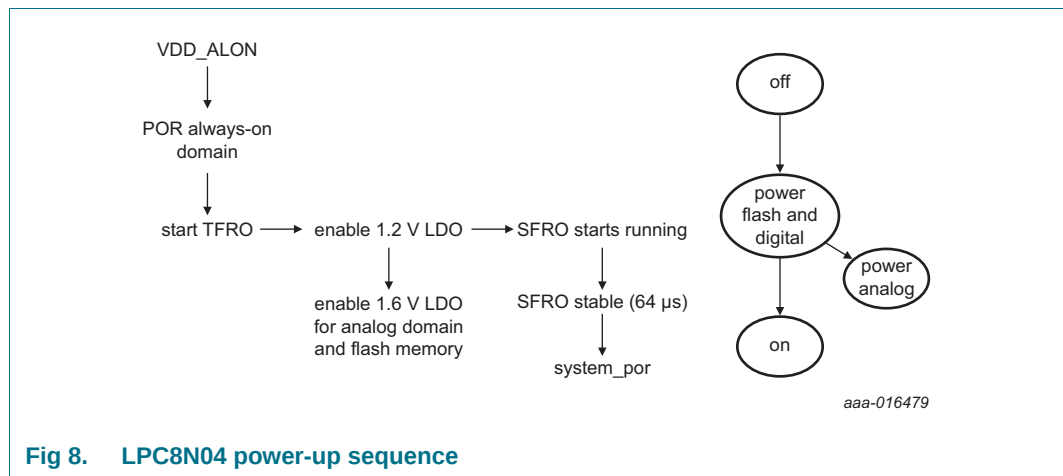
**Remark:** When running without a battery, energy harvesting is limited to 2 MHz system clock.

**Table 5. State transition events for DEEPSLEEP to ACTIVE**

| Event                 | Description                                                       |
|-----------------------|-------------------------------------------------------------------|
| RESETN                | reset asserted                                                    |
| RTC event             | if the timer reaches preset value                                 |
| Watchdog              | watchdog issues interrupt or reset                                |
| WAKEUP                | signal on WAKEUP pin                                              |
| RF field              | RF field is detected, potential NFC command input (if set in PMU) |
| Start logic interrupt | one of the enabled start logic interrupts is asserted             |

**Table 6. State transition events for DEEPPDN to ACTIVE**

| Event     | Description                                                       |
|-----------|-------------------------------------------------------------------|
| RESETN    | reset asserted                                                    |
| RTC event | if the timer reaches preset value                                 |
| WAKEUP    | signal on WAKEUP pin (when enabled)                               |
| RF field  | RF field is detected, potential NFC command input (if set in PMU) |



**Fig 8. LPC8N04 power-up sequence**

#### 8.4.1.1 Applying power to the PCB/system with battery for the first time

To support long shelf life without draining the battery, the LPC8N04 is not connected to an external supply pin until  $\overline{\text{RESET}}$  pin is asserted and de-asserted or the NFC field is present. Once the  $\overline{\text{RESET}}$  or the NFC field is applied, the LPC8N04 is powered.

#### 8.4.2 Power Management Unit (PMU)

The Power Management Unit (PMU) partly resides in the digital power domain and partly in the always-on domain. The PMU controls the sleep, deep sleep and deep power-down modes and the power flow to the different internal circuit blocks. Five general-purpose registers in the PMU can be used to retain data during deep power-down mode. These registers are located in the always-on domain. The PMU also raises a BOD interrupt, if necessary, if VDD\_ALON drops below 1.8 V.

The power to the different APB analog slaves is controlled through a power-down configuration register.

The power control register selects whether an ARM Cortex-M0+ controlled power-down mode (sleep mode or deep sleep mode) or the deep power-down mode is entered. It also provides the flags for sleep or deep-sleep modes and deep power-down mode respectively. In addition, it contains the overrides for the power source selection.

## 8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is a part of the ARM Cortex-M0+. The tight integration of the processor core and NVIC enables fast processing of interrupts, dramatically reducing the interrupt latency.

### 8.5.1 Features

- NVIC that is a part of the ARM Cortex-M0+
- Tightly coupled interrupt controller provides low interrupt latency
- Controls system exceptions and peripheral interrupts
- Four programmable interrupt priority levels with hardware priority level masking
- Software interrupt generation

### 8.5.2 Interrupt sources

[Table 7](#) lists the interrupt sources for each peripheral function. Each peripheral device may have one or more interrupt lines to the NVIC. Each line may represent more than one interrupt source. There is no significance or priority about which line is connected where, except for certain standards from ARM.

**Table 7. Connection of interrupt source to the NVIC**

| Exception number | Vector offset | Function                       | Flags                                                                                              |
|------------------|---------------|--------------------------------|----------------------------------------------------------------------------------------------------|
| 0 to 12          | -             | start logic wake-up interrupts | each interrupt connected to a PIO0 input pin serves as wake-up from deep-sleep mode <sup>[1]</sup> |
| 13               | -             | RFID/NFC                       | RFID/NFC access detected/command received/read acknowledge                                         |
| 14               | -             | RTC on/off timer               | RTC on/off timer event interrupt                                                                   |
| 15               | -             | I <sup>2</sup> C-bus           | Slave Input (SI) (state change)                                                                    |
| 16               | -             | CT16B                          | 16-bit timer                                                                                       |
| 17               | -             | PMU                            | power from NFC field detected                                                                      |
| 18               | -             | CT32B                          | 32-bit timer                                                                                       |
| 19               | -             | BOD                            | brownout detection (power drop)                                                                    |
| 20               | -             | SPI/SSP                        | TX FIFO half empty/RX FIFO half full/<br>RX time-out/RX overrun                                    |
| 21               | -             | TSENS                          | temperature sensor end of conversion/low threshold/<br>high threshold                              |
| 22 to 25         | -             | -                              | RESERVED                                                                                           |
| 26               | -             | WDT                            | watchdog interrupt (WDINT)                                                                         |
| 27               | -             | flash                          | flash memory                                                                                       |
| 28               | -             | EEPROM                         | EEPROM memory                                                                                      |
| 29 to 30         | -             | -                              | RESERVED                                                                                           |
| 31               | -             | PIO0                           | GPIO interrupt status of port 0                                                                    |

[1] Interrupt 0 to 10 correspond to PIO0\_0 to PIO0\_10; interrupt 11 corresponds to RFID/NFC external access; interrupt 12 corresponds to the RTC on/off timer.

## 8.6 I/O configuration

The I/O configuration registers control the electrical characteristics of the pads. The following features are programmable:

- Pin function
- Internal pull-up/pull-down resistor or bus keeper function
- Low-pass filter
- I<sup>2</sup>C-bus mode for pads hosting the I<sup>2</sup>C-bus function

The IOCON registers control the function (GPIO or peripheral function), the input mode, and the hysteresis of all PIO0\_m pins. In addition, the I<sup>2</sup>C-bus pins can be configured for different I<sup>2</sup>C-bus modes.

The FUNC bits in the IOCON registers can be set to GPIO (FUNC = 000) or to a peripheral function. If the pins are GPIO pins, the GPIO0DIR registers determine whether the pin is configured as an input or output. For any peripheral function, the pin direction is controlled automatically depending on the functionality of the pin. The GPIO0DIR registers have no effect on peripheral functions.

### 8.6.1 PIO0 pin mode

The MODE bits in the IOCON register allow the selection of on-chip pull-up or pull-down resistors for each pin, or to select the repeater mode. The possible on-chip resistor configurations are pull-up enabled, pull-down enabled, or no pull-up/pull-down. The default value is no pull-up or pull-down enabled. The repeater mode enables the pull-up resistor when the pin is at logic 1, and enables the pull-down resistor when the pin is at logic 0. This mode causes the pin to retain its last known state if it is configured as an input and is not driven externally. The state retention is not applicable to the deep power-down mode. Repeater mode is typically used to prevent a pin from floating when it is temporarily not driven. Allowing it to float could potentially use significant power.

### 8.6.2 PIO0 I<sup>2</sup>C-bus mode

If the FUNC bits of registers PIO0\_4 and PIO0\_5 select the I<sup>2</sup>C-bus function, the I<sup>2</sup>C-bus pins can be configured for different I<sup>2</sup>C-bus modes:

- Standard mode/fast mode I<sup>2</sup>C-bus with input glitch filter (including an open-drain output according to the I<sup>2</sup>C-bus specification)
- Standard open-drain I/O functionality without input filter

### 8.6.3 PIO0 current source mode

PIO0\_3, PIO0\_7, PIO0\_10 and PIO0\_11 are high-source pads that can deliver up to 20 mA to the load. These PIO pins can be set to either digital mode or analog current sink mode. In digital mode, the output voltage of the pad switches between VSS and VDD. In analog current drive mode, the output current sink switches between the values set by the ILO and IHI bits. The maximum pad voltage is limited to 5 V.

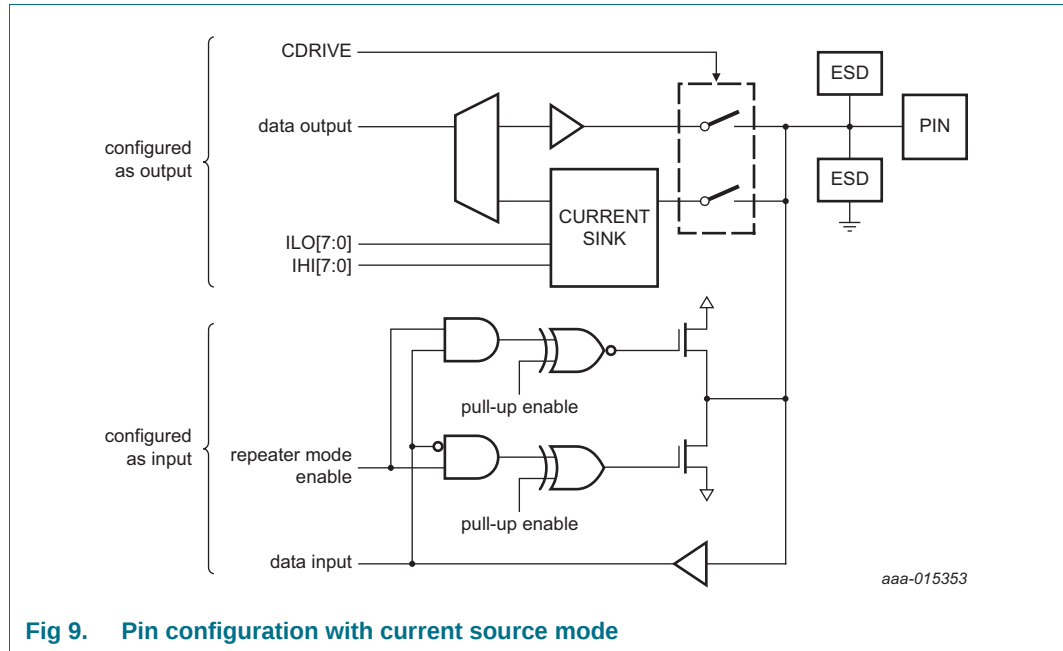


Fig 9. Pin configuration with current source mode

## 8.7 Fast general-purpose parallel I/O

The GPIO registers control device pins that are not connected to a specific peripheral function. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC8N04 uses accelerated GPIO functions:

- GPIO registers are on the ARM Cortex-M0+ I/O bus for fastest possible single-cycle I/O timing
- An entire port value can be written in one instruction
- Mask, set, and clear operations are supported for the entire port

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin.

### 8.7.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation
- Direction control of individual bits
- After reset, all I/Os default to GPIO inputs without pull-up or pull-down resistors. The I<sup>2</sup>C-bus true open-drain pins PIO0\_4 and PIO0\_5 and the SWD pins PIO0\_10 and PIO0\_11 are exceptions
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin
- Direction (input/output) can be set and cleared individually
- Pin direction bits can be toggled

## 8.8 I<sup>2</sup>C-bus controller

### 8.8.1 Features

Standard I<sup>2</sup>C-bus compliant interfaces may be configured as master, slave, or master/slave.

- Arbitration is handled between simultaneously transmitting masters without corruption of serial data on the bus
- Programmable clock allows adjustment of I<sup>2</sup>C-bus transfer rates
- Data transfer is bidirectional between masters and slaves
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization is used as a handshake mechanism to suspend and resume serial transfer
- Supports standard mode (100 kbit/s) and fast mode (400 kbit/s)
- Optional recognition of up to four slave addresses
- Monitor mode allows observing all I<sup>2</sup>C-bus traffic, regardless of slave address
- The I<sup>2</sup>C-bus can be used for test and diagnostic purposes
- The I<sup>2</sup>C-bus contains a standard I<sup>2</sup>C-bus compliant interface with two pins
- Possibility to wake up LPC8N04 on matching I<sup>2</sup>C-bus slave address

### 8.8.2 General description

Two types of data transfers are possible on the I<sup>2</sup>C-bus, depending on the state of the direction bit (R/W):

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the slave address). The slave then returns an acknowledge bit. The slave then transmits the data bytes to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. As a repeated START condition is also the beginning of the next serial transfer, the I<sup>2</sup>C-bus is not released.

The I<sup>2</sup>C-bus interface is byte oriented and has four operating modes: master transmitter mode, master receiver mode, slave transmitter mode and slave receiver mode.

The I<sup>2</sup>C-bus interface is completely I<sup>2</sup>C-bus compliant, supporting the ability to power off the LPC8N04 independent of other devices on the same I<sup>2</sup>C-bus.

The I<sup>2</sup>C-bus interface requires a minimum 2 MHz system clock to operate in normal mode, and 8 MHz for fast mode.

### 8.8.3 I<sup>2</sup>C-bus pin description

Table 8. I<sup>2</sup>C-bus pin description

| Pin | Type | Description                       |
|-----|------|-----------------------------------|
| SDA | I/O  | I <sup>2</sup> C-bus serial data  |
| SCL | I/O  | I <sup>2</sup> C-bus serial clock |

The I<sup>2</sup>C-bus pins must be configured through the PIO0\_4 and PIO0\_5 registers for standard mode or fast mode. The I<sup>2</sup>C-bus pins are open-drain outputs and fully compatible with the I<sup>2</sup>C-bus specification.

## 8.9 SPI controller

### 8.9.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments Synchronous Serial Interface (SSI), and National Semiconductor Microwire buses
- Synchronous serial communication
- Supports master or slave operation
- Eight-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

### 8.9.2 General description

The SPI/SSP is a Synchronous Serial Port (SSP) controller capable of operation on an SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 bits to 16 bits of bidirectional data flowing between master and slave. In practice, often only one of these two data flows carries meaningful data.

### 8.9.3 Pin description

Table 9. SPI pin description

| Pin name | Type | Interface pin SPI | SSI              | Microwire        | Description               |
|----------|------|-------------------|------------------|------------------|---------------------------|
| SCLK     | I/O  | SCLK              | CLK              | SK               | serial clock              |
| SSEL     | I/O  | SSEL              | FS               | CS               | frame sync/slave select   |
| MISO     | I/O  | MISO              | DR (M)<br>DX (S) | SI (M)<br>SO (S) | master input slave output |
| MOSI     | I/O  | MOSI              | DX (M)<br>DR (S) | SO (M)<br>SI (S) | master output slave input |

#### Pin detailed descriptions

**Serial clock** — SCK/CLK/SK is a clock signal used to synchronize the transfer of data. The master drives the clock signal and the slave receives it. When SPI/SSP interface is used, the clock is programmable to be active HIGH or active LOW, otherwise it is always active HIGH. SCK only switches during a data transfer. At any other time, the SPI/SSP interface either stays in its inactive state or is not driven (remains in high-impedance state).

**Frame sync/slave select** — When the SPI/SSP interface is a bus master, it drives this signal to an active state before the start of serial data. It then releases it to an inactive state after the data has been sent. The active state can be HIGH or LOW depending upon the selected bus and mode. When the SPI/SSP interface is a bus slave, this signal qualifies the presence of data from the master according to the protocol in use.

When there is only one master and slave, the master signals, frame sync or slave select, can be connected directly to the corresponding slave input. When there are multiple slaves, further qualification of frame sync/slave select inputs is normally necessary to prevent more than one slave from responding to a transfer.

**Master Input Slave Output (MISO)** — The MISO signal transfers serial data from the slave to the master. When the SPI/SSP is a slave, it outputs serial data on this signal. When the SPI/SSP is a master, it clocks in serial data from this signal. It does not drive this signal and leaves it in a high-impedance state when the SPI/SSP is a slave and not selected by FS/SSEL.

**Master Output Slave Input (MOSI)** — The MOSI signal transfers serial data from the master to the slave. When the SPI/SSP is a master, it outputs serial data on this signal. When the SPI/SSP is a slave, it clocks in serial data from this signal.

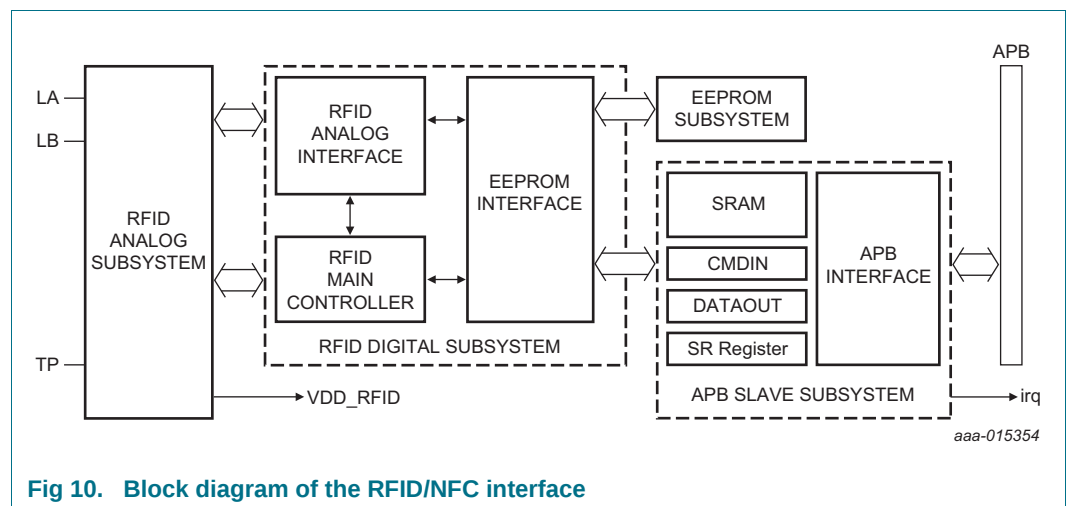
## 8.10 RFID/NFC communication unit

### 8.10.1 Features

- ISO/IEC14443A part 1 to part 3 compatible
- MIFARE (Ultralight) EV1 compatible
- NFC Forum Type 2 compatible
- Easy interfacing with standard user memory space READ/WRITE commands
- Passive operation possible

### 8.10.2 General description

The RFID/NFC interface allows communication using 13.56 MHz proximity signaling.



**Fig 10. Block diagram of the RFID/NFC interface**

The CMDIN, DATAOUT, Status Register (SR) and SRAM are mapped in the user memory space of the RFID core. The RFID READ and WRITE commands allow wireless communication to this shared memory.

Messages can be in raw mode (user proprietary protocol) or formatted according to NFC forum type 2 NDEF messaging and ISO/IEC 11073.

## 8.11 16-bit timer

### 8.11.1 Features

One 16-bit timer with a programmable 16-bit prescaler.

- Timer operation
- Four 16-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
- Up to two CT16B external outputs corresponding to the match registers with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match
- Up to two match registers can be configured as Pulse Width Modulation (PWM) allowing the use of up to two match outputs as single edge controlled PWM outputs

### 8.11.2 General description

The peripheral clock (PCLK), which is derived from the system clock, clocks the timer. The timer can optionally generate interrupts or perform other actions at specified timer values based on four match registers. The peripheral clock is provided by the system clock.

Each timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, four match registers can be used to provide a single-edge controlled PWM output on the match output pins. The use of the match registers that are not pinned out to control the PWM cycle length is recommended.

## 8.12 32-bit timer

### 8.12.1 Features

One 32-bit timer with a programmable 32-bit prescaler.

- Timer operation
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match

- Stop timer on match with optional interrupt generation
- Reset timer on match with optional interrupt generation
- Up to two CT32B external outputs corresponding to the match registers with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match
- Up to two match registers can be configured as PWM allowing the use of up to two match outputs as single edge controlled PWM outputs

### 8.12.2 General description

The peripheral clock (PCLK), which is derived from the system clock, clocks the timer. The timer can optionally generate interrupts or perform other actions at specified timer values based on four match registers. The peripheral clock is provided by the system clock.

Each timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, four match registers can be used to provide a single-edge controlled PWM output on the match output pins. Use of the match registers that are not pinned out to control the PWM cycle length is recommended.

## 8.13 WatchDog Timer (WDT)

If the microcontroller enters an erroneous state, the purpose of the WatchDog Timer (WDT) is to reset it within a reasonable amount of time.

When enabled, if the user program fails to feed (or reload) the WDT within a predetermined amount of time, the WDT generates a system reset.

### 8.13.1 Features

- If not periodically reloaded, it internally resets the microcontroller
- Debug mode
- Enabled by software but requires a hardware reset or a WDT reset/interrupt to be disabled
- If enabled, incorrect/incomplete feed sequence causes reset/interrupt
- Flag to indicate WDT reset
- Programmable 24-bit timer with internal prescaler
- Selectable time period from  $(\text{TWDCLK} \times 256 \times 4)$  to  $(\text{TWDCLK} \times 2^{24} \times 4)$  in multiples of  $\text{TWDCLK} \times 4$
- The WDT clock (WDCLK) source is a 2 MHz clock derived from the SFRO, or the external clock as set by the SYSCLKCTRL register

### 8.13.2 General description

The WDT consists of a divide by 4 fixed prescaler and a 24-bit counter. The clock is fed to the timer via a prescaler. The timer decrements when clocked. The minimum value by which the counter is decremented is 0xFF. Setting a value lower than 0xFF causes 0xFF to be loaded in the counter. Hence the minimum WDT interval is  $(TWDCLK \times 256 \times 4)$  and the maximum is  $(TWDCLK \times 2^{24} \times 4)$ , in multiples of  $(TWDCLK \times 4)$ .

## 8.14 System tick timer

### 8.14.1 Features

- Simple 24-bit timer
- Uses dedicated exception vector
- Clocked internally by the system clock or the system clock divided by two

### 8.14.2 General description

The SYSTICK timer is a part of the Cortex-M0+. The SYSTICK timer can be used to generate a fixed periodic interrupt for use by an operating system or other system. Since the SYSTICK timer is a part of the Cortex-M0+, it facilitates porting of software by providing a standard timer available on Cortex-M0+ based devices. The SYSTICK timer can be used for management software.

Refer to the *Cortex-M0+ Devices - Generic User Guide* ([Ref. 2](#)) for details.

## 8.15 Real-Time Clock (RTC) timer

### 8.15.1 Features

The Real-Time Clock (RTC) block two counters:

1. A countdown timer generating a wake-up signal when it expires
2. A continuous counter that counts seconds since power-up or the last system reset

The countdown timer runs on a low speed clock and runs in an always-on power domain. The delay, as well as a clock tuning prescaler, can be configured via the APB bus. The RTC countdown timer generates both the deep power-down wake-up signal and the RTC interrupt signal (wake-up interrupt 12). The deep power-down wake-up signal is always generated, while the interrupt can be masked according to the settings in the RTCIMSC register.

### 8.15.2 General description

The RTC module consists of two parts:

1. The RTC core module, implementing the RTC timers themselves. This module runs in the always-on VDD\_ALON domain.
2. The AMBA APB slave interface. This module allows configuration of the RTC core via an APB bus. This module runs in the switched power domain.

## 8.16 Temperature sensor

### 8.16.1 Features

The temperature sensor block measures the chip temperature, and outputs a raw value or a calibrated value in Kelvin.

### 8.16.2 General description

The temperature is measured using a high-precision, zoom-ADC. The analog part is able to measure a highly temperature-dependent  $X = V_{be} / \Delta V_{be}$ <sup>1</sup>. It determines the value of X by first applying a coarse search (successive approximation), and then a sigma-delta in a limited range.

## 8.17 Serial Wire Debug (SWD)

The debug functions are integrated into the ARM Cortex-M0+. Serial Wire Debug (SWD) functions are supported. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watchpoints.

- Supports ARM SWD mode
- Direct debug access to all memories, registers, and peripherals
- No target resources are required for the debugging session
- Four breakpoints. Four instruction breakpoints that can also be used to remap instruction addresses for code patches. Two data comparators that can be used to remap addresses for patches to literal values
- Two data watchpoints that can also be used as triggers

## 8.18 On-chip flash memory

The LPC8N04 contains a 32 kB flash memory of which 30 kB can be used as program and data memory.

The flash is organized in 32 sectors of 1 kB. Each sector consists of 16 rows of  $16 \times 32$ -bit words.

### 8.18.1 Reading from flash

Reading is done via the AHB interface. The memory is mapped on the bus address space as a contiguous address space. Memory data words are seen on the bus using a little endian arrangement.

### 8.18.2 Writing to flash

Writing to flash means copying a word of data over the AHB to the page buffer of the flash. It does not actually program the data in the memory array. This programming is done by subsequent erase and program cycles.

1.  $V_{be}$  is the base-emitter voltage of a bipolar transistor. Basically, the temperature sensor measures the voltage drop over a diode formed by the base-emitter junction of a bipolar transistor. It compares the  $V_{be}$  at different current levels (from which follows the  $\Delta V_{be}$ ).

### 8.18.3 Erasing/programming flash

Erasing and programming are separate operations. Both are possible only on memory sectors that are unprotected and unlocked. Protect/lock information is stored inside the memory itself, so the controller is not aware of protection status. Therefore, if a program/erase operation is performed on a protected or locked sector, it does not flag an error.

**Protection** — At exit from reset, all sectors are protected against accidental modification. To allow modification, a sector must be unprotected. It can then be protected again after that the modification is performed.

**Locking** — Each flash sector has a lock bit. Lock bits can be set but cannot be cleared. Locked sectors cannot be erased and reprogrammed.

### 8.19 On-chip SRAM

The LPC8N04 contains a total of 8 kB on-chip SRAM memory configured as  $256 \times 2 \times 4 \times 32$  bit.

### 8.20 On-chip EEPROM

The LPC8N04 contains a 4 kB EEPROM. This EEPROM is organized in 64 rows of  $32 \times 16$ -bit words. Of these rows, the last four contain calibration and test data and are locked. This data is either used by the bootloader after reset, or made accessible to the application via firmware Application Programming Interface (API).

#### 8.20.1 Reading from EEPROM

Reading is done via the AHB interface. The memory is mapped on the bus address space, as a contiguous address space. Memory data words are seen on the bus using a little endian arrangement.

#### 8.20.2 Writing to EEPROM

Erasing and programming is performed, as a single operation, on one or more words inside a single page.

Previous write operations have transferred the data to be programmed into the memory page buffer. The page buffer tracks which words were written to (offset within the page only). Words not written to, retain their previous content.

## 9. Limiting values

**Table 10. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol    | Parameter                       | Conditions                                               | Min   | Max   | Unit |
|-----------|---------------------------------|----------------------------------------------------------|-------|-------|------|
| $V_{DD}$  | supply voltage                  |                                                          | −0.5  | +3.6  | V    |
| $V_I$     | input voltage                   | normal PIO pads ( $V_{DD} = 0.6$ V)                      | −0.5  | +3.6  | V    |
|           |                                 | high-source PIO pads                                     | −0.5  | +5.5  | V    |
|           |                                 | LA/LB pads                                               | −0.5  | +5.5  | V    |
| $I_{DD}$  | supply current                  | per supply pin                                           | -     | 100   | mA   |
| $I_{SS}$  | ground supply current           | per supply pin                                           | -     | 100   | mA   |
| $I_{lu}$  | latch-up current                | I/O; $-0.5V_{DD} < V_I < +1.5V_{DD}$ ;<br>$T_j < 125$ °C | -     | 100   | mA   |
| $T_{stg}$ | storage temperature             |                                                          | −40   | +125  | °C   |
| $T_j$     | junction temperature            |                                                          | -     | 125   | °C   |
| $P_{tot}$ | total power dissipation         |                                                          | -     | 1     | W    |
| $V_{ESD}$ | electrostatic discharge voltage | human body model; all pins                               | −2000 | +2000 | V    |
|           |                                 | charged device model; all pins                           | −500  | +500  | V    |

## 10. Static characteristics

**Table 11. Static characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ , unless otherwise stated.

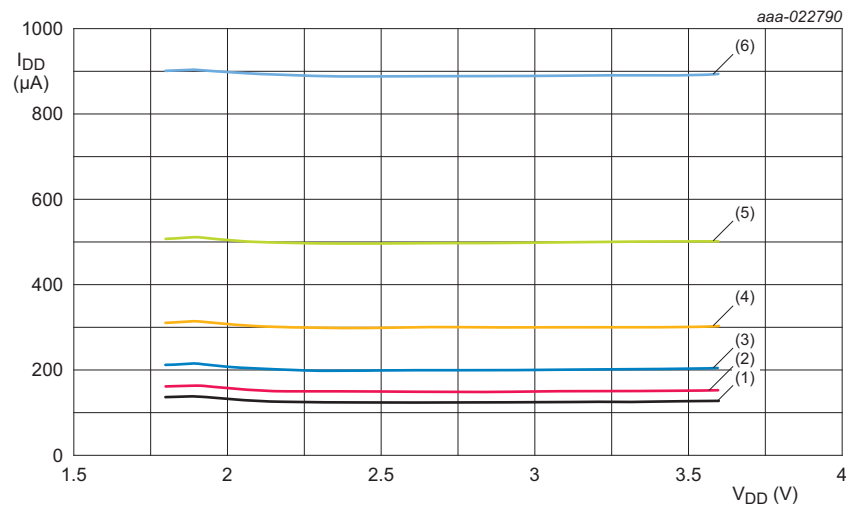
| Symbol                    | Parameter                      | Conditions                                             | Min                   | Typ   | Max                   | Unit |
|---------------------------|--------------------------------|--------------------------------------------------------|-----------------------|-------|-----------------------|------|
| Supply pins               |                                |                                                        |                       |       |                       |      |
| V <sub>DD</sub>           | supply voltage                 |                                                        | 1.72                  | 3.0   | 3.60                  | V    |
| I <sub>DD</sub>           | supply current                 | voltage and clock frequency <a href="#">[1]</a>        | -                     | -     | -                     | μA   |
| I <sub>L(off)</sub>       | off-state leakage current      |                                                        | -                     | -     | 50                    | nA   |
| I <sub>DD(pd)</sub>       | power-down mode supply current | deep power-down mode                                   | -                     | 3     | -                     | μA   |
| Standard GPIO pins        |                                |                                                        |                       |       |                       |      |
| V <sub>IH</sub>           | HIGH-level input voltage       |                                                        | 0.7 × V <sub>DD</sub> | -     | -                     | V    |
| V <sub>IL</sub>           | LOW-level input voltage        |                                                        | -                     | -     | 0.3 × V <sub>DD</sub> | V    |
| V <sub>hys</sub>          | hysteresis voltage             |                                                        | 0.4                   | -     | -                     | V    |
| R <sub>pd</sub>           | pull-down resistance           |                                                        | -                     | 72    | -                     | kΩ   |
| R <sub>pu</sub>           | pull-up resistance             |                                                        | -                     | 73    | -                     | kΩ   |
| I <sub>S</sub>            | source current                 | HIGH-level V <sub>DD</sub> = 1.8 V <a href="#">[2]</a> | -                     | 2     | -                     | mA   |
|                           |                                | HIGH-level V <sub>DD</sub> = 3.6 V <a href="#">[2]</a> | -                     | 8     | -                     | mA   |
|                           |                                | LOW-level V <sub>DD</sub> = 1.8 V <a href="#">[2]</a>  | -                     | 4     | -                     | mA   |
|                           |                                | LOW-level V <sub>DD</sub> = 3.6 V <a href="#">[2]</a>  | -                     | 16    | -                     | mA   |
| High-drive GPIO pins      |                                |                                                        |                       |       |                       |      |
| I <sub>S</sub>            | source current                 | HIGH-level V <sub>DD</sub> = 1.8 V <a href="#">[3]</a> | 4                     | -     | 6                     | mA   |
|                           |                                | HIGH-level V <sub>DD</sub> = 3.6 V <a href="#">[3]</a> | 13                    | -     | 18                    | mA   |
|                           |                                | LOW-level V <sub>DD</sub> = 1.8 V <a href="#">[3]</a>  | 5.5                   | -     | 8                     | mA   |
|                           |                                | LOW-level V <sub>DD</sub> = 3.6 V <a href="#">[3]</a>  | 22                    | -     | 32                    | mA   |
| I <sup>2</sup> C-bus pins |                                |                                                        |                       |       |                       |      |
| I <sub>S</sub>            | source current                 | LOW-level V <sub>DD</sub> = 1.8 V <a href="#">[4]</a>  | 2                     | -     | 8.5                   | mA   |
|                           |                                | LOW-level V <sub>DD</sub> = 3.6 V <a href="#">[4]</a>  | 9.5                   | -     | 38                    | mA   |
| Brownout detect           |                                |                                                        |                       |       |                       |      |
| V <sub>trip(bo)</sub>     | brownout trip voltage          | falling V <sub>DD</sub>                                | -                     | 1.8   | -                     | V    |
|                           |                                | rising V <sub>DD</sub>                                 | -                     | 1.875 | -                     | V    |
| V <sub>hys</sub>          | hysteresis voltage             |                                                        | -                     | 75    | -                     | mV   |
| General                   |                                |                                                        |                       |       |                       |      |
| R <sub>pu(int)</sub>      | internal pull-up resistance    | on pin RESETN                                          | -                     | 100   | -                     | kΩ   |
| C <sub>ext</sub>          | external capacitance           | on pin RESETN                                          | -                     | -     | 1                     | nF   |

[1] See [Figure 11](#).

[2] PIO0\_0, PIO0\_1, PIO0\_2, PIO0\_6, PIO0\_8, PIO0\_9.

[3] PIO0\_3, PIO0\_7, PIO0\_10, PIO0\_11.

[4] PIO0\_4, PIO0\_5.



Plot of  $I_{DD} / V_{DD}$  when ARM running a while-1 loop in normal mode, no NFC field present.

- (1) System clock = 250 kHz
- (2) System clock = 500 kHz
- (3) System clock = 1 MHz
- (4) System clock = 2 MHz
- (5) System clock = 4 MHz
- (6) System clock = 8 MHz

Fig 11. Active current consumption

Table 12. Temperature sensor characteristics

| Symbol         | Parameter                      | Conditions       | Min  | Typ | Max  | Unit        |
|----------------|--------------------------------|------------------|------|-----|------|-------------|
| $I_{CC(pd)}$   | power-down mode supply current | TSENS disabled   | -    | -   | 1    | nA          |
| $I_{stb}$      | standby current                | TSENS enabled    | -    | 6   | 7    | $\mu A$     |
| $I_{CC(oper)}$ | operating supply current       | TSENS converting | -    | 10  | 12   | $\mu A$     |
| $T_{acc}$      | temperature accuracy           |                  | -1.5 | -   | +1.5 | $^{\circ}C$ |

**Note:** The absolute accuracy is valid for the factory calibration of the temperature sensor. The sensor can be user-calibrated to reach higher accuracy.

Table 13. Antenna input characteristics

| Symbol | Parameter         | Conditions          | Min | Typ   | Max | Unit |
|--------|-------------------|---------------------|-----|-------|-----|------|
| $C_i$  | input capacitance | <a href="#">[1]</a> | -   | 50    | -   | pF   |
| $f_i$  | input frequency   |                     | -   | 13.56 | -   | MHz  |

[1]  $T_{amb} = 22^{\circ}C$ ,  $f = 13.56$  MHz, RMS voltage between LA and LB = 1.5 V.

Table 14. EEPROM characteristics

| Symbol          | Parameter           | Conditions              | Min | Typ | Max | Unit |
|-----------------|---------------------|-------------------------|-----|-----|-----|------|
| $t_{ret(data)}$ | data retention time | $T_{amb} = 22^{\circ}C$ | 10  | -   | -   | year |

## 11. Dynamic characteristics

### 11.1 I/O pins

**Table 15. I/O dynamic characteristics**

These characteristics apply to standard port pins and RESETN pin.

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

| Symbol | Parameter | Conditions               | Min | Typ | Max | Unit |
|--------|-----------|--------------------------|-----|-----|-----|------|
| $t_r$  | rise time | pin configured as output | 3.0 | -   | 5.0 | ns   |
| $t_f$  | fall time | pin configured as output | 2.5 | -   | 5.0 | ns   |

### 11.2 I<sup>2</sup>C-bus

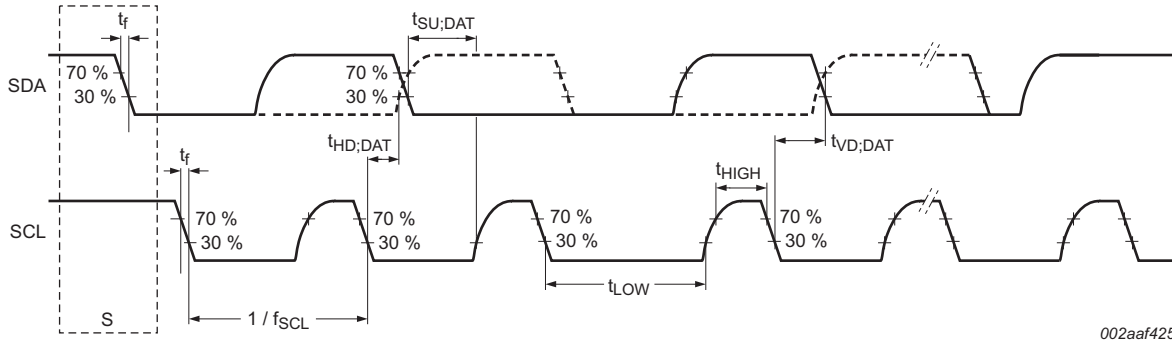
**Table 16. I<sup>2</sup>C-bus dynamic characteristics**

See UM10204 - I<sup>2</sup>C-bus specification and user manual (Ref. 3) for details.

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ <sup>[1]</sup>; see the timing diagram in Figure 12.

| Symbol       | Parameter                             | Conditions                         | Min                   | Typ | Max | Unit          |
|--------------|---------------------------------------|------------------------------------|-----------------------|-----|-----|---------------|
| $f_{SCL}$    | SCL clock frequency                   | standard mode                      | 0                     | -   | 100 | kHz           |
|              |                                       | fast mode                          | 0                     | -   | 400 | kHz           |
| $t_f$        | fall time of both SDA and SCL signals | standard mode <sup>[2][3][4]</sup> | -                     | -   | 300 | ns            |
|              |                                       | fast mode <sup>[2][3][4]</sup>     | $20 + 0.1 \times C_b$ | -   | 300 | ns            |
| $t_{LOW}$    | LOW period of the SCL clock           | standard mode                      | 4.7                   | -   | -   | $\mu\text{s}$ |
|              |                                       | fast mode                          | 1.3                   | -   | -   | $\mu\text{s}$ |
| $t_{HIGH}$   | HIGH period of the SCL clock          | standard mode                      | 4.0                   | -   | -   | $\mu\text{s}$ |
|              |                                       | fast mode                          | 0.6                   | -   | -   | $\mu\text{s}$ |
| $t_{HD,DAT}$ | data hold time                        | standard mode <sup>[2][5][6]</sup> | 0                     | -   | -   | $\mu\text{s}$ |
|              |                                       | fast mode <sup>[2][5][6]</sup>     | 0                     | -   | -   | $\mu\text{s}$ |
| $t_{SU,DAT}$ | data set-up time                      | standard mode <sup>[7][8]</sup>    | 250                   | -   | -   | ns            |
|              |                                       | fast mode <sup>[7][8]</sup>        | 100                   | -   | -   | ns            |

- [1] Parameters are valid over operating temperature range unless otherwise specified.
- [2] A device must internally provide a hold time of at least 300 ns for the SDA signal (regarding the  $V_{IH(min)}$  of the SCL signal). The hold time is to bridge the undefined region of the falling edge of SCL.
- [3]  $C_b$  = total capacitance of one bus line in pF.
- [4] The maximum  $t_f$  for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage  $t_f$  is specified at 250 ns. It allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_f$ .
- [5]  $t_{HD,DAT}$  is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
- [6] The maximum  $t_{HD,DAT}$  could be 3.45  $\mu\text{s}$  and 0.9  $\mu\text{s}$  for standard mode and fast mode. However, it must be less than the maximum of  $t_{VD,DAT}$  or  $t_{VD,ACK}$  by a transition time (see Ref. 3). Only meet this maximum if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
- [7]  $t_{SU,DAT}$  is the data set-up time that is measured against the rising edge of SCL; applies to data in transmission and the acknowledge.
- [8] A fast mode I<sup>2</sup>C-bus device can be used in a standard-mode I<sup>2</sup>C-bus system but it must meet the requirement  $t_{SU,DAT} = 250$  ns. This requirement is automatically the case if the device does not stretch the LOW period of the SCL signal. If it does, it must output the next data bit to the SDA line  $t_{r(max)} + t_{SU,DAT} = 1000 + 250 = 1250$  ns before the SCL line is released. This procedure is in accordance with the standard-mode I<sup>2</sup>C-bus specification. Also, the acknowledge timing must meet this set-up time.



S = START condition

Fig 12. I<sup>2</sup>C-bus pins clock timing

### 11.3 SPI interfaces

Table 17. Dynamic characteristics of SPI pins in SPI mode

| Symbol            | Parameter              | Conditions                                    | Min                         | Typ | Max                          | Unit |
|-------------------|------------------------|-----------------------------------------------|-----------------------------|-----|------------------------------|------|
| <b>SPI master</b> |                        |                                               |                             |     |                              |      |
| $t_{cy(clk)}$     | clock cycle time       | full-duplex mode [1]                          | 50                          | -   | -                            | ns   |
|                   |                        | when only transmitting [1]                    | 40                          | -   | -                            | ns   |
| $t_{SU;DAT}$      | data set-up time       | $2.4\text{ V} \leq V_{DD} < 3.6\text{ V}$ [2] | 15                          | -   | -                            | ns   |
|                   |                        | $2.0\text{ V} \leq V_{DD} < 2.4\text{ V}$ [2] | 20                          | -   | -                            | ns   |
|                   |                        | $1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$ [2] | 24                          | -   | -                            | ns   |
| $t_{HD;DAT}$      | data hold time         | [2]                                           | 0                           | -   | -                            | ns   |
| $t_{V(Q)}$        | data output valid time | [2]                                           | -                           | -   | 10                           | ns   |
| $t_{H(Q)}$        | data output hold time  | [2]                                           | 0                           | -   | -                            | ns   |
| <b>SPI slave</b>  |                        |                                               |                             |     |                              |      |
| $T_{cy(PCLK)}$    | PCLK cycle time        | [3][4]                                        | 0                           | -   | -                            | ns   |
| $t_{HD;DAT}$      | data hold time         | [3][4]                                        | $3 \times T_{cy(PCLK)} + 4$ | -   | -                            | ns   |
| $t_{V(Q)}$        | data output valid time | [3][4]                                        | -                           | -   | $3 \times T_{cy(PCLK)} + 11$ | ns   |
| $t_{H(Q)}$        | data output hold time  | [3][4]                                        | -                           | -   | $2 \times T_{cy(PCLK)} + 5$  | ns   |

[1]  $t_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSPVSR) / f_{main}$ . The clock cycle time derived from the SPI bit rate  $t_{cy(clk)}$  is a function of:

- the main clock frequency  $f_{main}$
- the SPI peripheral clock divider (SSPCLKDIV)
- the SPI SCR parameter (specified in the SSP0CR0 register)
- the SPI CPSPVSR parameter (specified in the SPI clock prescale register)

[2]  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ .

[3]  $t_{cy(clk)} = 12 \times T_{cy(PCLK)}$ .

[4]  $T_{amb} = 25\text{ }^{\circ}\text{C}$  for normal voltage supply:  $V_{DD} = 3.3\text{ V}$ .

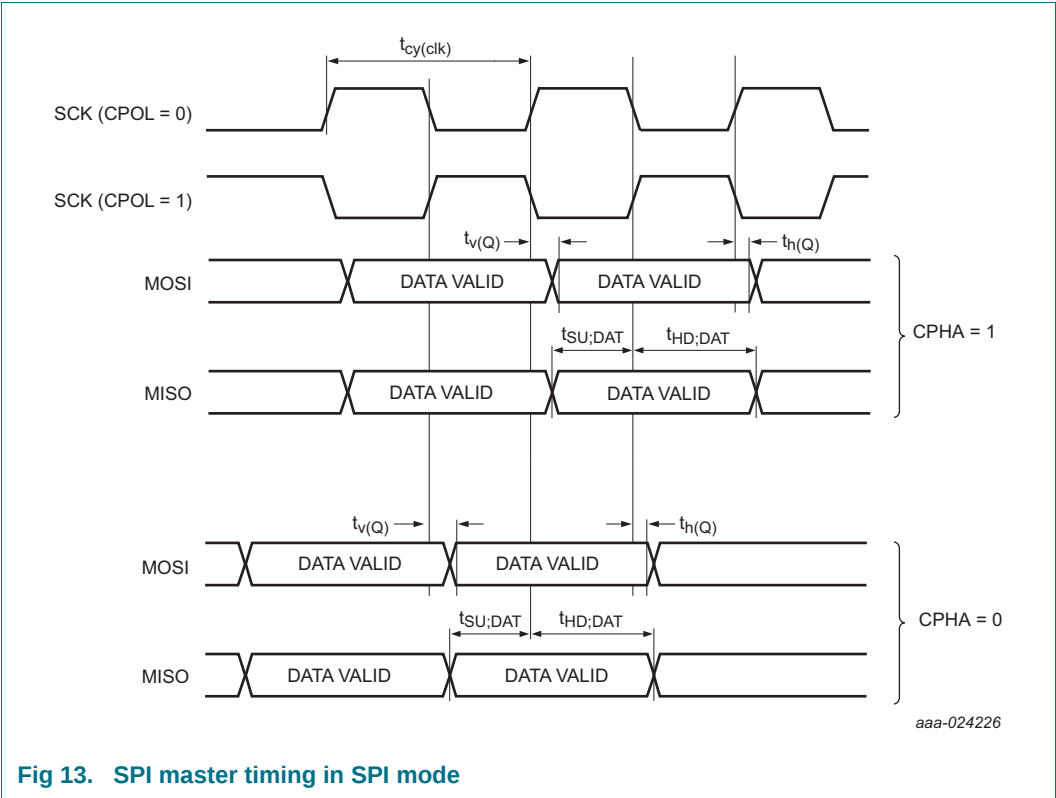


Fig 13. SPI master timing in SPI mode

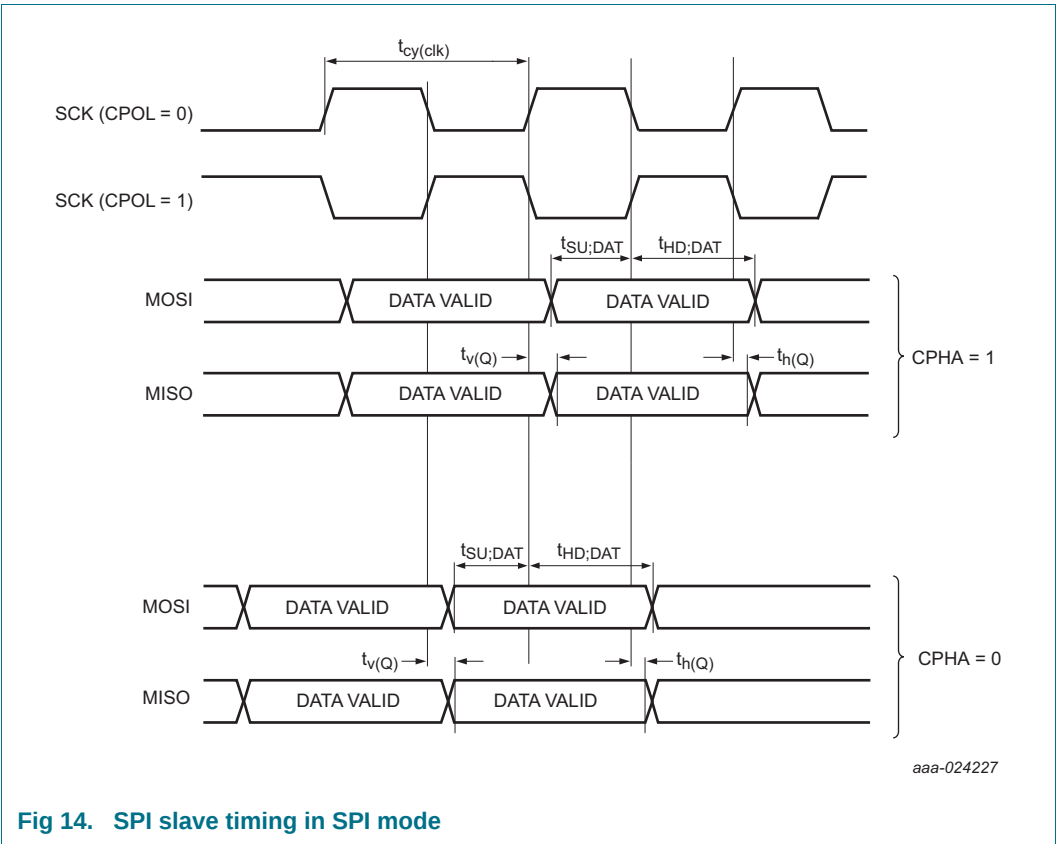


Fig 14. SPI slave timing in SPI mode

12. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads;  
24 terminals; body 4 x 4 x 0.85 mm

SOT616-3

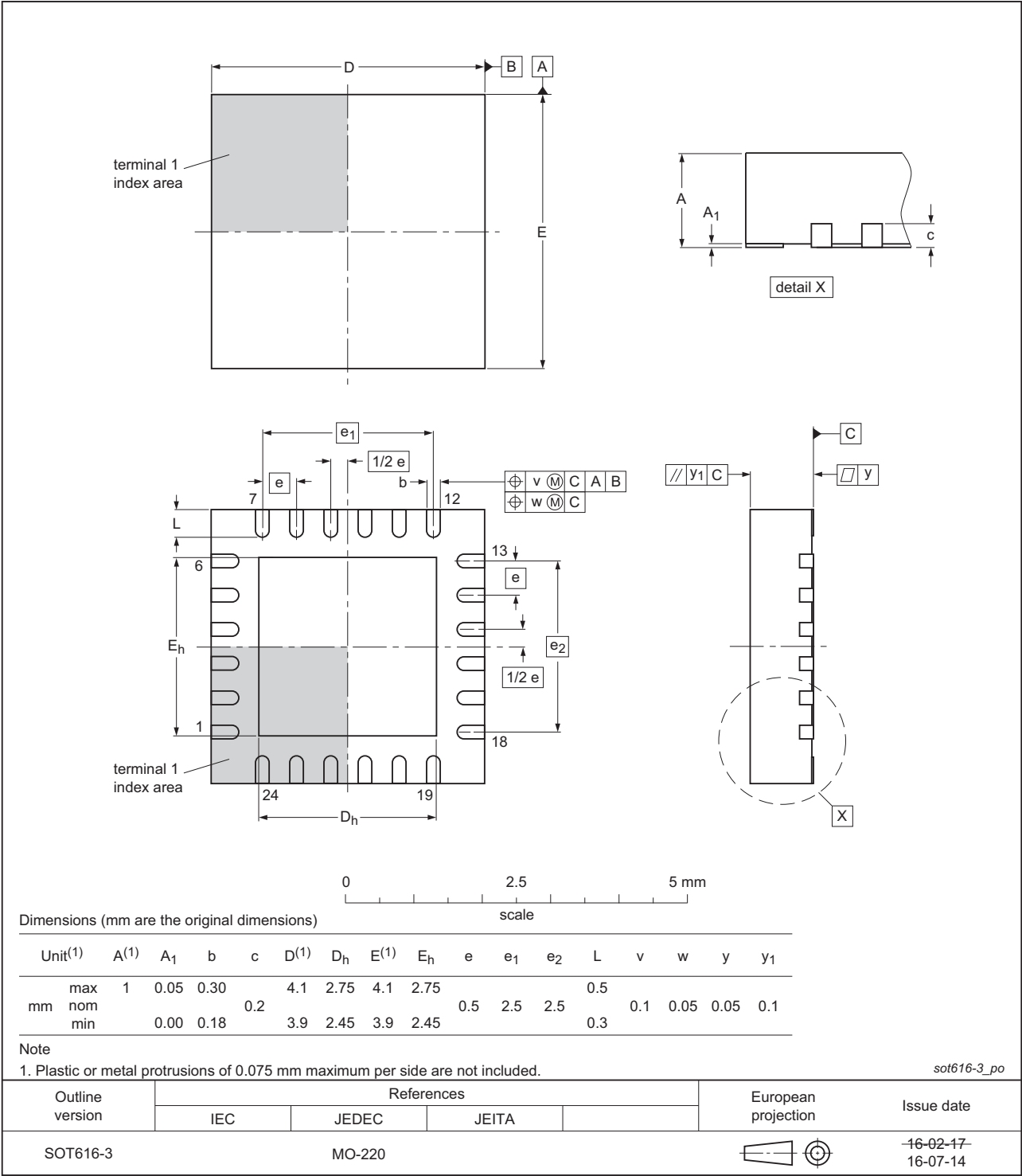


Fig 15. HVQFN24 package outline

## 13. Abbreviations

Table 18. Abbreviations

| Acronym          | Description                                         |
|------------------|-----------------------------------------------------|
| ADC              | Analog-to-Digital Converter                         |
| AHB              | Advanced High-performance Bus                       |
| AMBA             | Advanced Microcontroller Bus Architecture           |
| APB              | Advanced Peripheral Bus                             |
| API              | Application Programming Interface                   |
| ARM              | Advanced RISC Machine                               |
| BOD              | BrownOut Detection                                  |
| CGU              | Clock Generator Unit                                |
| EEPROM           | Electrically Erasable Programmable Read-Only Memory |
| GPIO             | General Purpose Input Output                        |
| I <sup>2</sup> C | Inter-Integrated Circuit                            |
| LDO              | Low DropOut                                         |
| MISO             | Master Input Slave Output                           |
| MOSI             | Master Output Slave Input                           |
| NDEF             | NFC Data Exchange Format                            |
| NFC              | Near Field Communication                            |
| NVIC             | Nested Vectored Interrupt Controller                |
| PMU              | Power Management Unit                               |
| POR              | Power-On Reset                                      |
| PWM              | Pulse Width Modulation                              |
| RFID             | Radio Frequency Identification                      |
| RISC             | Reduced Instruction Set Computer                    |
| RTC              | Real-Time Clock                                     |
| SFRO             | System Free-Running Oscillator                      |
| SI               | Slave Input                                         |
| SO               | Slave Output                                        |
| SPI              | Serial Peripheral Interface                         |
| SR               | Status Register                                     |
| SSI              | Synchronous Serial Interface                        |
| SSP              | Synchronous Serial Port                             |
| SWD              | Serial Wire Debug                                   |
| TFRO             | Timer Free-Running Oscillator                       |
| WDT              | WatchDog Timer                                      |

## 14. References

---

- [1] **DDI0484C\_cortex\_m0p\_r0p1\_trm** — Cortex-M0+ Devices - Technical Reference Manual
- [2] **DUI0662B\_cortex\_m0p\_r0p1\_dgug** — Cortex-M0+ Devices - Generic User Guide
- [3] **UM10204** — I<sup>2</sup>C-bus specification and user manual

## 15. Revision history

**Table 19. Revision history**

| Document ID   | Release date                                                                                                                                                                                                                                                                                                                                                                        | Data sheet status  | Change notice | Supersedes    |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------|---------------|
| LPC8N04 v.1.4 | 20180608                                                                                                                                                                                                                                                                                                                                                                            | Product data sheet | -             | LPC8N04 v.1.3 |
| Modification: | <ul style="list-style-type: none"> <li>Updated <a href="#">Section 2 “Features and benefits”</a>: Added text: OTA firmware update using Secondary Bootloader (SBL) library (See TN00040: LPC8N04: Encrypted Over the Air (OTA) Firmware update using NFC). OTA firmware update available on Boot ROM version 0.14.</li> <li>Updated <a href="#">Section 5 “Marking”</a>.</li> </ul> |                    |               |               |
| LPC8N04 v.1.3 | 20180301                                                                                                                                                                                                                                                                                                                                                                            | Product data sheet | -             | LPC8N04 v.1.2 |
| Modification: | <ul style="list-style-type: none"> <li>Changed title to Cortex-M0+.</li> </ul>                                                                                                                                                                                                                                                                                                      |                    |               |               |
| LPC8N04 v.1.2 | 20180301                                                                                                                                                                                                                                                                                                                                                                            | Product data sheet | -             | LPC8N04 v.1.1 |
| Modification: | <ul style="list-style-type: none"> <li>Added a remark to Section 8.4.1 “System power architecture”: When running without a battery, energy harvesting is limited to 2 MHz system clock.</li> </ul>                                                                                                                                                                                  |                    |               |               |
| LPC8N04 v.1.1 | 20171211                                                                                                                                                                                                                                                                                                                                                                            | Product data sheet | -             | LPC8N04 v.1.0 |
| Modification: | <ul style="list-style-type: none"> <li>Added text to Section 2 “Features and benefits”: Energy harvesting functionality to power the LPC8N04.</li> </ul>                                                                                                                                                                                                                            |                    |               |               |
| LPC8N04 v.1.0 | 20171012                                                                                                                                                                                                                                                                                                                                                                            | Product data sheet | -             | -             |

## 16. Legal information

### 16.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 16.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 16.4 Licenses

### Purchase of NXP ICs with NFC technology

Purchase of an NXP Semiconductors IC that complies with one of the Near Field Communication (NFC) standards ISO/IEC 18092 and ISO/IEC 21481 does not convey an implied license under any patent right infringed by implementation of any of those standards. Purchase of NXP Semiconductors IC does not include a license to any NXP patent (or other IP right) covering combinations of those products with other products, whether hardware or software.

## 16.5 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**MIFARE** — is a trademark of NXP B.V.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP B.V.

## 17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 18. Tables

---

|           |                                                 |    |
|-----------|-------------------------------------------------|----|
| Table 1.  | Ordering information                            | 3  |
| Table 2.  | Marking codes                                   | 3  |
| Table 3.  | Pad allocation table of the HVQFN24 package     | 5  |
| Table 4.  | Pad description of the HVQFN24 package          | 6  |
| Table 5.  | IC power states                                 | 12 |
| Table 6.  | State transition events for DEEPSLEEP to ACTIVE | 13 |
| Table 7.  | State transition events for DEEPPDN to ACTIVE   | 13 |
| Table 8.  | Connection of interrupt source to the NVIC      | 14 |
| Table 9.  | I <sup>2</sup> C-bus pin description            | 18 |
| Table 10. | SPI pin description                             | 18 |
| Table 11. | Limiting values                                 | 25 |
| Table 12. | Static characteristics                          | 26 |
| Table 13. | Temperature sensor characteristics              | 27 |
| Table 14. | Antenna input characteristics                   | 27 |
| Table 15. | EEPROM characteristics                          | 27 |
| Table 16. | I/O dynamic characteristics                     | 28 |
| Table 17. | I <sup>2</sup> C-bus dynamic characteristics    | 28 |
| Table 18. | Dynamic characteristics of SPI pins in SPI mode | 29 |
| Table 19. | Abbreviations                                   | 32 |
| Table 20. | Revision history                                | 33 |

## 19. Figures

---

|         |                                                      |    |
|---------|------------------------------------------------------|----|
| Fig 1.  | LPC8N04 block diagram . . . . .                      | 4  |
| Fig 2.  | Pad configuration HVQFN24 . . . . .                  | 5  |
| Fig 3.  | LPC8N04 memory map . . . . .                         | 8  |
| Fig 4.  | LPC8N04 clock generator block diagram . . . . .      | 9  |
| Fig 5.  | LPC8N04 power architecture . . . . .                 | 11 |
| Fig 6.  | PMU state transition diagram . . . . .               | 12 |
| Fig 7.  | LPC8N04 power-up sequence . . . . .                  | 13 |
| Fig 8.  | Pin configuration with current source mode . . . . . | 16 |
| Fig 9.  | Block diagram of the RFID/NFC interface . . . . .    | 19 |
| Fig 10. | Active current consumption . . . . .                 | 27 |
| Fig 11. | I <sup>2</sup> C-bus pins clock timing . . . . .     | 29 |
| Fig 12. | SPI master timing in SPI mode . . . . .              | 30 |
| Fig 13. | SPI slave timing in SPI mode . . . . .               | 30 |
| Fig 14. | HVQFN24 package outline . . . . .                    | 31 |

## 20. Contents

|          |                                                                            |          |           |                                          |           |
|----------|----------------------------------------------------------------------------|----------|-----------|------------------------------------------|-----------|
| <b>1</b> | <b>General description</b> . . . . .                                       | <b>1</b> | 8.13      | WatchDog Timer (WDT) . . . . .           | 21        |
| <b>2</b> | <b>Features and benefits</b> . . . . .                                     | <b>2</b> | 8.13.1    | Features . . . . .                       | 21        |
| <b>3</b> | <b>Applications</b> . . . . .                                              | <b>3</b> | 8.13.2    | General description . . . . .            | 22        |
| <b>4</b> | <b>Ordering information</b> . . . . .                                      | <b>3</b> | 8.14      | System tick timer . . . . .              | 22        |
| <b>5</b> | <b>Marking</b> . . . . .                                                   | <b>3</b> | 8.14.1    | Features . . . . .                       | 22        |
| <b>6</b> | <b>Block diagram</b> . . . . .                                             | <b>4</b> | 8.14.2    | General description . . . . .            | 22        |
| <b>7</b> | <b>Pinning information</b> . . . . .                                       | <b>5</b> | 8.15      | Real-Time Clock (RTC) timer . . . . .    | 22        |
| 7.1      | Pinning . . . . .                                                          | 5        | 8.15.1    | Features . . . . .                       | 22        |
| 7.1.1    | HVQFN24 package . . . . .                                                  | 5        | 8.15.2    | General description . . . . .            | 22        |
| <b>8</b> | <b>Functional description</b> . . . . .                                    | <b>7</b> | 8.16      | Temperature sensor . . . . .             | 23        |
| 8.1      | ARM Cortex-M0+ core . . . . .                                              | 7        | 8.16.1    | Features . . . . .                       | 23        |
| 8.2      | Memory map . . . . .                                                       | 7        | 8.16.2    | General description . . . . .            | 23        |
| 8.3      | System configuration . . . . .                                             | 8        | 8.17      | Serial Wire Debug (SWD) . . . . .        | 23        |
| 8.3.1    | Clock generation . . . . .                                                 | 8        | 8.18      | On-chip flash memory . . . . .           | 23        |
| 8.3.2    | Reset . . . . .                                                            | 9        | 8.18.1    | Reading from flash . . . . .             | 23        |
| 8.4      | Power management . . . . .                                                 | 10       | 8.18.2    | Writing to flash . . . . .               | 23        |
| 8.4.1    | System power architecture . . . . .                                        | 10       | 8.18.3    | Erasing/programming flash . . . . .      | 24        |
| 8.4.1.1  | Applying power to the PCB/system with battery for the first time . . . . . | 13       | 8.19      | On-chip SRAM . . . . .                   | 24        |
| 8.4.2    | Power Management Unit (PMU) . . . . .                                      | 13       | 8.20      | On-chip EEPROM . . . . .                 | 24        |
| 8.5      | Nested Vectored Interrupt Controller (NVIC) . . . . .                      | 14       | 8.20.1    | Reading from EEPROM . . . . .            | 24        |
| 8.5.1    | Features . . . . .                                                         | 14       | 8.20.2    | Writing to EEPROM . . . . .              | 24        |
| 8.5.2    | Interrupt sources . . . . .                                                | 14       | <b>9</b>  | <b>Limiting values</b> . . . . .         | <b>25</b> |
| 8.6      | I/O configuration . . . . .                                                | 15       | <b>10</b> | <b>Static characteristics</b> . . . . .  | <b>26</b> |
| 8.6.1    | PIO0 pin mode . . . . .                                                    | 15       | <b>11</b> | <b>Dynamic characteristics</b> . . . . . | <b>28</b> |
| 8.6.2    | PIO0 I <sup>2</sup> C-bus mode . . . . .                                   | 15       | 11.1      | I/O pins . . . . .                       | 28        |
| 8.6.3    | PIO0 current source mode . . . . .                                         | 15       | 11.2      | I <sup>2</sup> C-bus . . . . .           | 28        |
| 8.7      | Fast general-purpose parallel I/O . . . . .                                | 16       | 11.3      | SPI interfaces . . . . .                 | 29        |
| 8.7.1    | Features . . . . .                                                         | 16       | <b>12</b> | <b>Package outline</b> . . . . .         | <b>31</b> |
| 8.8      | I <sup>2</sup> C-bus controller . . . . .                                  | 17       | <b>13</b> | <b>Abbreviations</b> . . . . .           | <b>32</b> |
| 8.8.1    | Features . . . . .                                                         | 17       | <b>14</b> | <b>References</b> . . . . .              | <b>33</b> |
| 8.8.2    | General description . . . . .                                              | 17       | <b>15</b> | <b>Revision history</b> . . . . .        | <b>34</b> |
| 8.8.3    | I <sup>2</sup> C-bus pin description . . . . .                             | 18       | <b>16</b> | <b>Legal information</b> . . . . .       | <b>35</b> |
| 8.9      | SPI controller . . . . .                                                   | 18       | 16.1      | Data sheet status . . . . .              | 35        |
| 8.9.1    | Features . . . . .                                                         | 18       | 16.2      | Definitions . . . . .                    | 35        |
| 8.9.2    | General description . . . . .                                              | 18       | 16.3      | Disclaimers . . . . .                    | 35        |
| 8.9.3    | Pin description . . . . .                                                  | 18       | 16.4      | Licenses . . . . .                       | 36        |
|          | Pin detailed descriptions . . . . .                                        | 18       | 16.5      | Trademarks . . . . .                     | 36        |
| 8.10     | RFID/NFC communication unit . . . . .                                      | 19       | <b>17</b> | <b>Contact information</b> . . . . .     | <b>36</b> |
| 8.10.1   | Features . . . . .                                                         | 19       | <b>18</b> | <b>Tables</b> . . . . .                  | <b>37</b> |
| 8.10.2   | General description . . . . .                                              | 19       | <b>19</b> | <b>Figures</b> . . . . .                 | <b>38</b> |
| 8.11     | 16-bit timer . . . . .                                                     | 20       | <b>20</b> | <b>Contents</b> . . . . .                | <b>39</b> |
| 8.11.1   | Features . . . . .                                                         | 20       |           |                                          |           |
| 8.11.2   | General description . . . . .                                              | 20       |           |                                          |           |
| 8.12     | 32-bit timer . . . . .                                                     | 20       |           |                                          |           |
| 8.12.1   | Features . . . . .                                                         | 20       |           |                                          |           |
| 8.12.2   | General description . . . . .                                              | 21       |           |                                          |           |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2018.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 8 June 2018

Document identifier: LPC8N04

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

[LPC8N04FHI24E](#) [LPC8N04FHI24Z](#)